SH-III/Electronics-302C-6(T)/19

B.Sc. Semester III (Honours) Examination, 2018-19

ELECTRONICS

Course ID : 31712 **Course Code : SHELC-302C-6(T)**

Course Title : Digital Electronics and Verilog (VHDL)

Time: 1 Hour 15 Minutes **Full Marks: 25**

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer *any three* of the following: 1×3=3

(a) What are minterm and maxterm?

(b) How many Half adders and Full adders will be required to add two 32-bit numbers?

(c) What is sequential logic circuit? Give one example.

(d) What is the difference between a decoder and a demultiplexer?

(e) Draw the logic circuit of 1-bit comparator.

(f) Mention the name of logic gate which is used as equality detector.

2. Answer *any three* of the following: 2×3=6

(a) What is sign magnitude representation? Represent $(-15)_{10}$ in this representation. 1+1=2

(b) What is 'Propagation delay time' and 'fan out' of a logic gate? 1+1=2

(c) What do you mean by 'Bipolar' and 'Unipolar' logic families? Give one example of each. 1+1=2

(d) Convert in standard SOP form— $Y = AB + A\bar{C} + BC$. 2

(e) What is shift register? Mention its two applications. 1+1=2

(f) What do you mean by self complementing codes? Name two self complementing codes. 1+1=2

3. Answer *any two* of the following: 5×2=10

(a) Perform the following:

(i) $(AF.B9)_{16} = (?)_8$

(ii) $(1011011)_2 = (?)_{Gray}$

(iii) $(459.23)_{10} = (?)_{xs3}$

(iv) $(776)_8 + (567)_8$

(v) $(106.45)_{10} = (?)_8$

(b) Perform the following:

(i) $(-5)_{10} + (-4)_{10}$ using 1's complement method.

(ii) $(15)_{10} - (21)_{10}$ using 2's complement method. 2½+2½=5

(c) Explain CMOS Inverter with proper circuit. Compare CMOS and TTL logic families. 3+2=5

(d) Draw the logic symbol of clocked R-S flip-flop and give its truth-table. How will you get D and T flip-flop from JK flip-flop? 2+2+1=5

Or,

What is Full subtractor? Write down its truth table. Implement a Full subtractor using Demultiplexer. 1+1+3=5

4. Answer *any one* of the following questions: 6×1=6

(a) Explain the working of a Half subtractor with logic diagram and truth table. Realize it using NOR gates only. 3+3=6

(b) Minimize the following expression using K-Map and realize using NOR gates only. f (P, Q, R, S,) = $\prod$ M (1, 4, 6, 9, 10, 11, 14, 15). 4+2=6

(c) Implement the following Boolean expression using multiplexer:

$Y = (A + B)\,(\overline{A} + B + C)\,(A + \overline{B})$ 6

Or,

Design MOD-10 counter using JK flip-flop and explain its operation in brief. Draw its timing diagram. 4+1+1=6

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